



Applications Note: SY8303

High Efficiency Fast Response, 3A, 40V Input Synchronous Step Down Regulator Preliminary Specification

General Description

The SY8303 develops a high efficiency synchronous step-down DC-DC converter capable of delivering 3A load current. The SY8303 operates over a wide input voltage range from 4.5V to 40V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

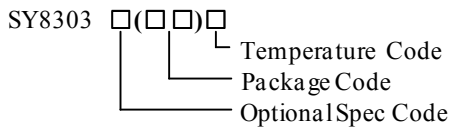
The SY8303 adopts peak current control scheme. The switching frequency is adjustable from 500kHz to 2.5MHz using an external resistor. The device also features ultra low quiescent operating to achieve high efficiency under light load. And the internal soft-start limits inrush current during power on.

SY8303 is available in TSOT23-8 package.

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 110/70 m Ω
- 4.5-40V input voltage range
- Internal compensation
- Internal 1ms soft-start limits the inrush current
- Adjustable switching frequency range: 500kHz to 2.5MHz
- 3A output current capability
- 1.5% 0.6V reference
- Low quiescent current
- Cycle-by-cycle peak current limitation
- Short circuit protection
- Thermal shutdown and auto recovery
- RoHS Compliant and Halogen Free
- Compact package: TSOT23-8

Ordering Information



Ordering Number	Package type	Note
SY8303AIC	TSOT23-8	--

Applications

- LCD-TV
- SetTop Box
- Notebook
- Storage
- High Power AP Router
- Networking

Typical Applications

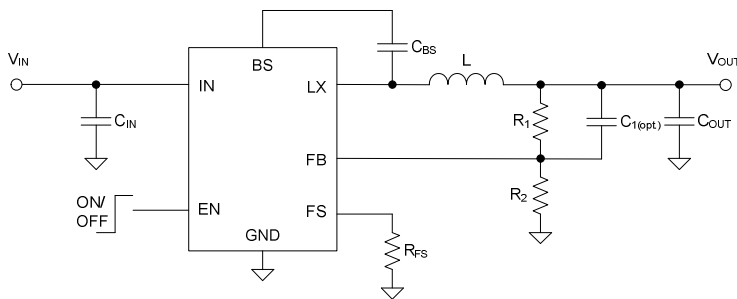


Figure 1. Schematic Diagram

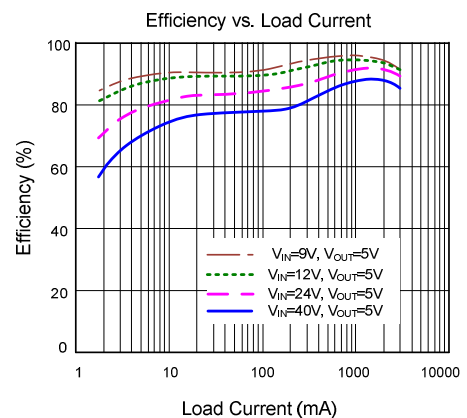
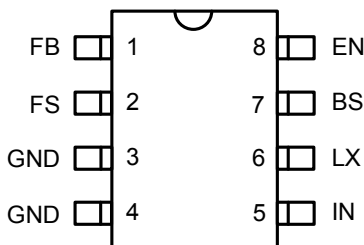


Figure 2. Efficiency vs. Load Current



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Pinout (top view)



Top Mark: **XDxyz** (Device code: XD, *x*=year code, *y*=week code, *z*=lot number code)

Pin Name	Pin Number	Pin Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6*(1+R1/R2)$
FS	2	Frequency programming pin. Connect a resistor to ground to program a switching frequency between 500kHz to 2.5MHz. The switching frequency equals to: $F_{sw}=10^5/R_{FS}$ kHz, where R_{FS} is in k Ω .
EN	8	Enable control. Pull high to turn on. Do not float.
GND	3,4	Ground pin.
IN	5	Input pin. Decouple this pin to GND pin with at least 4.7uF ceramic cap.
LX	6	Inductor pin. Connect this pin to the switching node of inductor.
BS	7	Boot-strap pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.

Absolute Maximum Ratings (Note 1)

IN to GND	-0.3V to 42V
LX, FB, EN, FS to GND	-0.3V to 42V
BS-LX	4V
Power Dissipation, PD @ T _A = 25°C TSOT23-8	TBD
Package Thermal Resistance (Note 2)	
θ_{JA}	TBD
θ_{JC}	TBD
Junction Temperature Range	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage	4.5V to 40V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C



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Electrical Characteristics

($V_{IN} = 12V$, $V_{OUT} = 5V$, $C_{OUT} = 47\mu F$, $T_A = 25^\circ C$, $I_{OUT} = 1A$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		40	V
Quiescent Current	I_Q	$I_{OUT}=0, V_{FB}=V_{REF}*105\%$			12	μA
Shutdown Current	I_{SHDN}	EN=0		1	2	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	$V_{FB}=V_{CC}$	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			110		m Ω
Bottom FET RON	$R_{DS(ON)2}$			70		m Ω
Top FET Current Limit	$I_{LIM, TOP}$		4		6.8	A
EN Low threshold	V_{ENL}		0.8			V
EN High Threshold	V_{ENH}				1.5	V
Input UVLO threshold	V_{UVLO}				4.2	V
UVLO hysteresis	V_{HYS}			0.2		V
Oscillator Frequency Program Range	F_{OSC}	$R_{FS}=200k$		0.5		MHz
Oscillator Frequency Accuracy			-15		15	% F_{OSC}
Soft-start Time	T_{SS}			1		ms
Min ON Time				80		ns
Min OFF Time				120		ns
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{SD,HYS}$			15		$^\circ C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

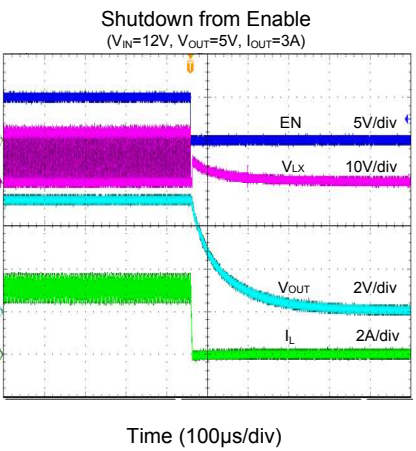
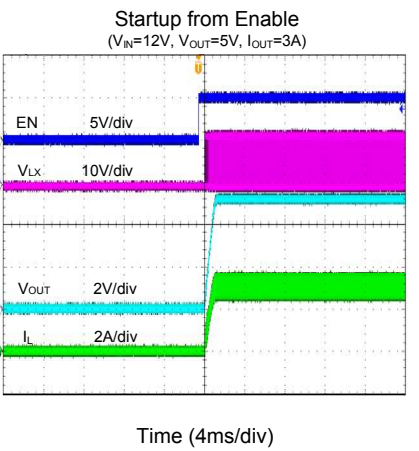
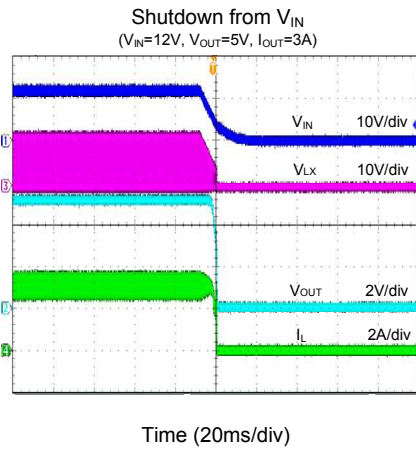
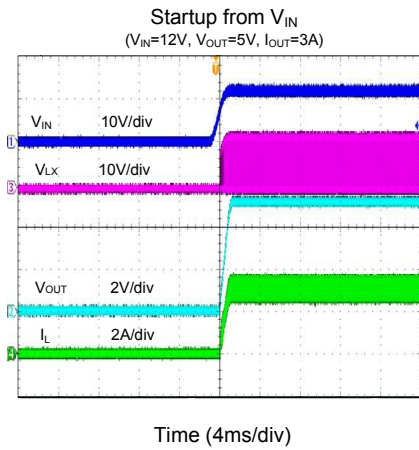
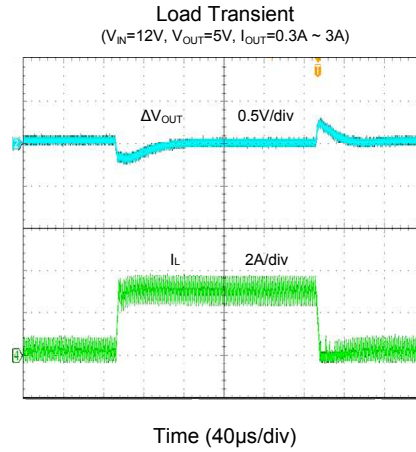
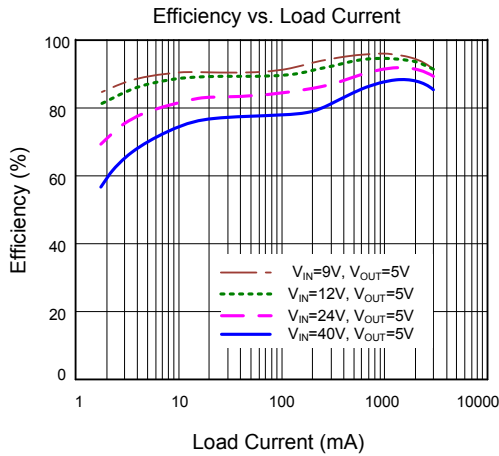
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective two layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.



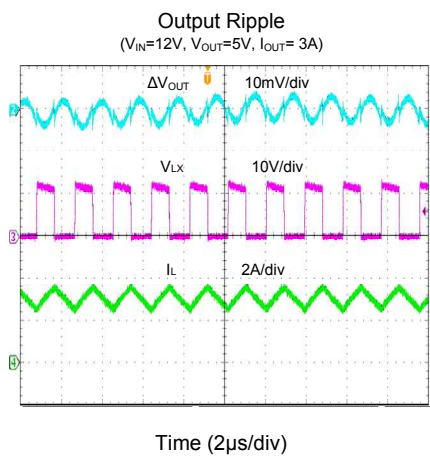
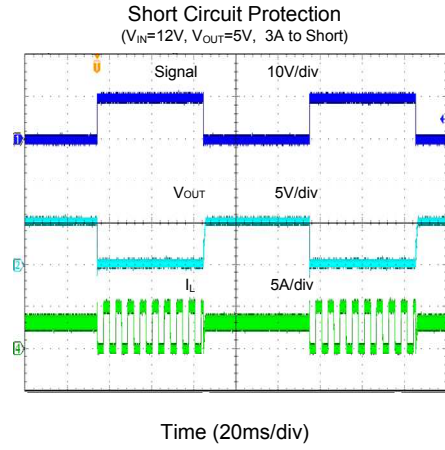
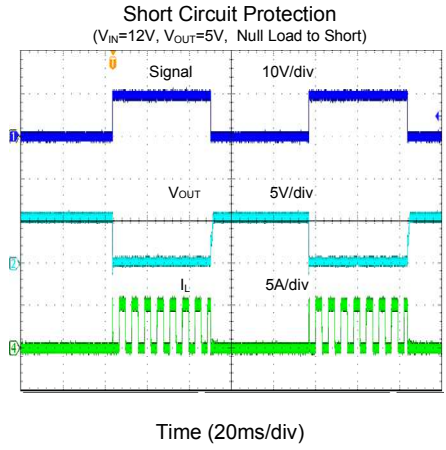
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Typical Performance Characteristics





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Operation

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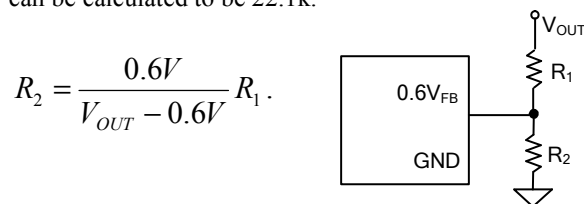
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Applications Information

Because of the high integration in the SY8303 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2 :

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2 . A value of between 10k Ω and 1M Ω is highly recommended for both resistors. If V_{out} is 3.3V, $R_1=100k$ is chosen, then using following equation, R_2 can be calculated to be 22.1k:



Input capacitor C_{IN} :

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND

pins. In this case, a 4.7uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT} :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22uF capacitance.

Output inductor L :

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where F_{sw} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8303 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

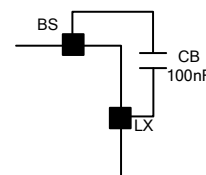
- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 50m\Omega$ to achieve a good overall efficiency.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.

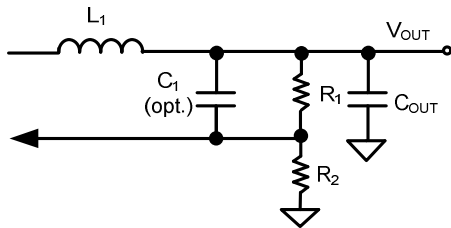




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Load Transient Considerations:

The SY8303 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic cap in parallel with R1 may further speed up the load transient response and it is recommended for applications with large load transient step requirements.



Layout Design:

The layout design of SY8303 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN} , L, R1 and R2.

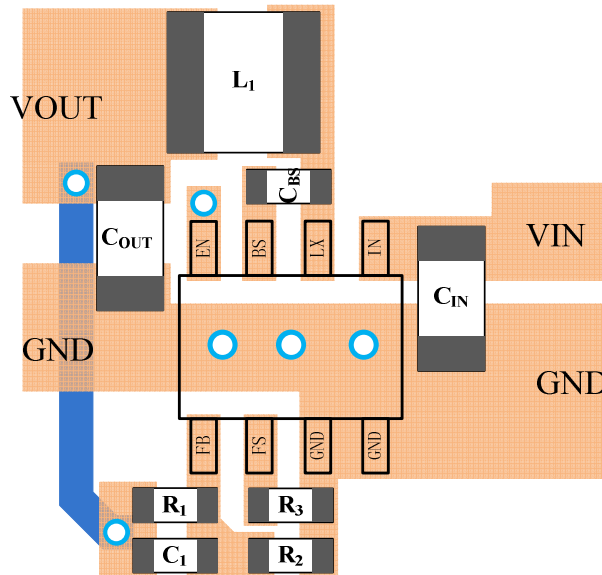
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

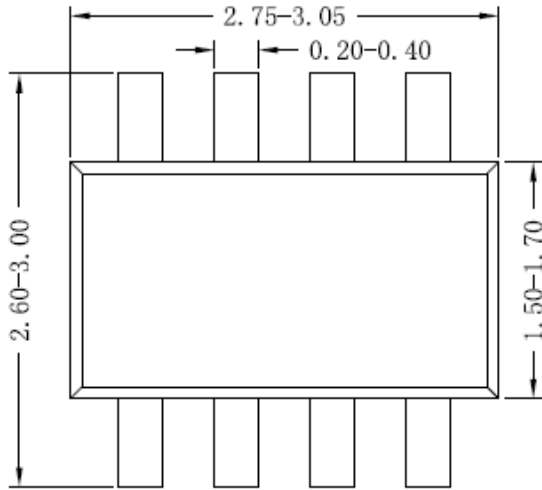
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.



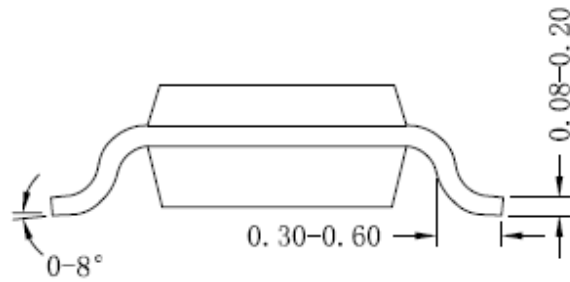


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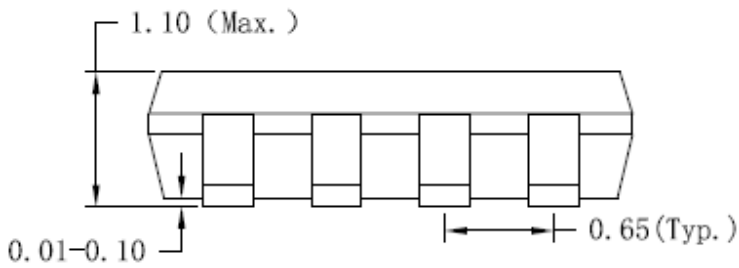
TSOT23-8 Package Outline Drawing



Top view



Side view A



Side view B

Notes: All dimension in MM and exclude mold flash & metal burr